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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,660	05/16/2001	Yasuhisa Shimazaki	XA-9472	1388

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EXAMINER

CHANG, DANIEL D

ART UNIT PAPER NUMBER

2819

DATE MAILED: 05/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/855,660

Applicant(s)

SHIMAZAKI ET AL.

Examiner

Daniel D. Chang

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 25-36 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14, 16, 18, 20-24 and 37-42 is/are rejected.
- 7) ☒ Claim(s) 13, 15, 17 and 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2819

***Acknowledgement***

Applicant's election of Group I comprising Claims 1-24 and 37-42 in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12, 14, 16, 18, 20-24, and 37-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al (US 5,583,457).

Regarding claims 1-12, 16, 20-24, and 39-42, Horiguchi et al. discloses, in figure 37, a semiconductor integrated circuit comprising:

a first logic gate (L41) using, as an operation power source, a first pair of a high potential (Vcl) and a low potential (Vsl); and

Art Unit: 2819

a second logic gate (L43) using, as an operation power source, a second pair of a high potential ( $V_{cc}$ ) and a low potential ( $V_{ss}$ ) having a potential difference larger than that of said first potential pair,

wherein a substrate potential of an MIS transistor (col. 3, lines 19+) in said first logic gate and that of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other (see substrates connected to  $V_{cc}$  and  $V_{ss}$ ), and

at least said first logic gate includes a p-channel type (MP41) and n-channel type (MN41) MIS transistors to which a substrate bias is applied in a reverse direction (see substrate respect to  $V_{cl}$  and  $V_{sl}$  on MP41 and MN41, respectively) by said substrate potential, and

at least said second logic gate includes a p-channel type (MP43) and n-channel type (MN43) MIS transistors to which a substrate bias is applied in a forward direction (see substrate respect to  $V_{cc}$  and  $V_{ss}$  on MP43 and MN43, respectively) by said substrate potential.

Regarding claims 14 and 18, Horiguchi et al. discloses, in figure 37, that the second high potential ( $V_{cc}$ ) is higher than the first high potential ( $V_{cl}$ ) and the second low potential ( $V_{ss}$ ) is lower than the first low potential ( $V_{sl}$ ), and said second high potential ( $V_{cc}$ ) is used as a high potential side substrate potential (see substrate of MP43), and said second low potential ( $V_{ss}$ ) is used as a low potential side substrate potential (see substrate of MN43).

Regarding claims 37 and 38, for the recitation, "a design data recording medium" with "data", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

***Allowable Subject Matter***

Claims 13, 15, 17, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Horiguchi et al., taken alone or in combination of other references, does not teach or fairly suggest a semiconductor integrated circuit comprising, among other things, a first substrate potential which is between the first and second high potentials and a second substrate potential which is between the first and second low potentials, as set forth in the claims.

***Conclusion***

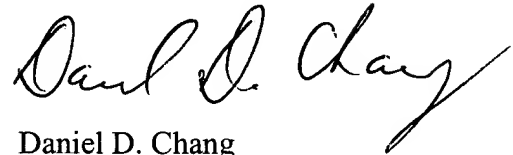
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Art Unit: 2819

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A handwritten signature in black ink, appearing to read "Daniel D. Chang". The signature is fluid and cursive, with a long horizontal stroke at the end.

Daniel D. Chang  
Examiner  
Art Unit 2819

DC  
May 6, 2002